UNIVERSITÀ DI PAVIA

Anno Accademico 2018/2019

DIGITAL IC DESIGN

Enrollment year	2018/2019
Academic year	2018/2019
Regulations	DM270
Academic discipline	ING-INF/01 (ELECTRONICS)
Department	DEPARTMENT OF ELECTRICAL,COMPUTER AND BIOMEDICAL ENGINEERING
Course	ELECTRONIC ENGINEERING
Curriculum	Microelectronics
Year of study	1°
Period	2nd semester (06/03/2019 - 14/06/2019)
ECTS	6
Lesson hours	70 lesson hours
Language	English
Activity type	WRITTEN AND ORAL TEST
Teacher	TORELLI GUIDO (titolare) - 6 ECTS
Prerequisites	Fundamentals of Logic Circuits, Basics of Electrical Engineering, Electronics, Basics of Digital Electronics, Basics of CMOS Logic Gates and Integrated Circuit Technology. Additional lectures can be agreed with interested students to refresh missing background prerequisites.
Learning outcomes	The main objective of the course is to provide the student with the basics of circuit design for combinational and sequential logic in CMOS technology and the operating principles of semiconductor memories. Theoretical lessons will be followed by practical classes in lecture theatre for detailed analysis and exercises, as well as by computer laboratory sessions, during which the student will use SPICE-based computer simulation to analyze basic digital circuit blocks. A few seminars on specific topics will also be provided. At the end of the course, the student is expected to be able to design and analyze basic digital circuit blocks and architectural solutions in CMOS technology as

	well as to evaluate their performance.
Course contents	Digital gates in CMOS technology Review of the MOS transistor. Review of inverter and combinational logic gates in CMOS technology. Transistor sizing of CMOS logic gates. Evaluation of rise time, fall time, and delay time of CMOS logic gates. Circuit performance estimation Estimation of parasitic electrical parameters (resistance, capacitance, inductance). Distributed RC effects of interconnect lines. Ring oscillator. Speed performance analysis of logic gates. Buffered structure for heavy capacitive loads. Power consumption estimation. Power consumption reduction techniques. Design margins. Sizing of interconnect lines. Pass transistor logic. Shrinking and technology scaling down. Circuit design in CMOS technology Design strategy for combinational logic. Dynamic CMOS logic; precharge logic; domino logic; clocked CMOS logic. Clocked sequential systems. Review of basic static memory elements (latch, flip-flop). Single-phase and two-phase timing. Dynamic memory elements. Synchronous systems. Pipeline architecture. Clock distribution in digital integrated circuits. Clock skew in synchronous systems. Remarks on low-power digital circuit design. Semiconductor memories Introduction to semiconductor memories. Memory types. Organization of a memory. Row and column address circuits. Review of volatile memories (static RAM, dynamic RAM). Content addressable memory (CAM). Non volatile memories: ROM, Flash memory; emerging non volatile memories: phase change memory. Charge pump based integrated voltage elevators.
Teaching methods	Lectures (hours/year in lecture theatre): 22 Practical class (hours/year in lecture theatre): 30 Practicals/Workshops and Seminars (hours/year in lecture theatre and computer lab): 18
Reccomended or required readings	N. H. E. Weste, K. Eshraghian . Principles of CMOS VLSI Design. A System Perspective. 2nd edition. Addison-Wesley Publishing Company, Reading, MA, USA, 1994. N. H. E. Weste, D. M. Harris. CMOS VLSI Design. A Circuits and Systems Perspective. 4th edition. Addison-Wesley, Boston, MA, USA, 2001. J. M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd Edition. Pearson Education, Inc. (Prentice Hall), Upper Saddle River, NJ, USA, 2003. S.-M. Kang, Y. Leblebici. CMOS Digital Integrated Circuits: Analysis and Design. The McGraw-Hill Companies, Inc., New York, NY, USA, 1996. For more details on CMOS digital integrated circuit design.

	Notes by the lecturer on specific topics will also be provided during the course.
Assessment methods	Written examination (exercises) and oral examination (theory). Relative weight: written examination 1/2, oral examination 1/2.
Further information	
Sustainable development goals - Agenda 2030	$lbl_legenda_sviluppo_sostenibile