UNIVERSITÀ DI PAVIA

Anno Accademico 2020/2021

DIGITAL IC DESIGN

Anno immatricolazione	2020/2021
Anno offerta	2020/2021
Normativa	DM270
SSD	ING-INF/01 (ELETTRONICA)
Dipartimento	DIPARTIMENTO DI INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE
Corso di studio	ELECTRONIC ENGINEERING
Curriculum	Microelectronics
Anno di corso	1°
Periodo didattico	Secondo Semestre (08/03/2021 - 14/06/2021)
Crediti	6
Ore	57 ore di attività frontale
Lingua insegnamento	English
Tipo esame	SCRITTO E ORALE CONGIUNTI
Docente	CABRINI ALESSANDRO (titolare) - 3 CFU CHIABRERA MICHELE - 3 CFU
Prerequisiti	Fundamentals of logic circuits, basics of electrical engineering (in particular, electrical networks), electronics, basics of digital electronics, basics of CMOS logic gates, and basics of integrated circuit technology. Additional lectures can be agreed with interested students to refresh missing background prerequisites.
Obiettivi formativi	The main objective of the course is to provide the student with the basics of circuit design for combinational and sequential logic in CMOS technology and the operating principles of semiconductor memories. At the end of the course, the student is expected to be able to design and analyze basic digital circuit blocks and architectural solutions in CMOS technology as well as to evaluate their performance and compare different implementations. The course is intended for students who plan to carry out their future professional activity in the areas of the design

	and application of digital and mixed analog-digital CMOS integrated circuits.
Programma e contenuti	Digital gates in CMOS technology Review of the MOS transistor. Review of ratioed and ratioless inverters, of inverter in CMOS technology, and of combinational logic gates in CMOS technology. Transistor sizing of CMOS logic gates. Evaluation of rise time, fall time, and delay time of CMOS inverter and logic gates . Performance estimation of digital CMOS circuits Estimation of parasitic electrical parameters (resistance, capacitance, inductance). Distributed RC effects of interconnect lines. Ring oscillator. Transfer gates in CMOS technology. Speed performance analysis of CMOS logic gates. Buffered structure for heavy capacitive loads. Design margins. Power consumption estimation. Power consumption reduction techniques. Sizing of interconnect lines. Pass transistor logic. Shrinking and technology scaling down. Circuit design in CMOS technology Design strategy for combinational logic. Dynamic CMOS logic; precharge logic; domino logic; clocked CMOS logic. Clocked sequential systems. Review of basic static memory elements (latch, flip-flop). Single-phase and two-phase timing. Dynamic memory elements. Synchronous digital systems. Pipeline architecture. Clock distribution in digital integrated circuits. Clock skew in synchronous systems. Remarks on power consumption optimization in CMOS digital circuit design. Semiconductor memories Introduction to semiconductor memories. Memory types. Organization of a memory. Row and column address circuits. Review of volatile memories (static RAM, dynamic RAM): elementary cells; write and read operations. Content addressable memory (CAM). Non volatile memories: ROM, Flash memory; emerging non volatile memories: phase change memory. Charge pump based integrated voltage elevators: operating principle; basic schemes.
Metodi didattici	Lectures (hours/year in lecture theatre): 22 Practical class (hours/year in lecture theatre): 30 Practicals/Workshops and Seminars (hours/year in lecture theatre and computer lab): 18 Classroom lectures will be given at the blackboard and/or by means of transparencies. Theoretical lectures will be followed by practical classes in lecture theatre for detailed analysis and exercises, as well as by computer laboratory sessions, during which the student will use SPICE-based computer simulation to analyze basic digital circuit blocks. A few seminars on specific topics will also be provided.
Testi di riferimento	N. H. E. Weste, K. Eshraghian . Principles of CMOS VLSI Design. A System Perspective. 2nd edition. Addison-Wesley Publishing Company, Reading, MA, USA, 1994. N. H. E. Weste, D. M. Harris. CMOS VLSI Design. A Circuits and Systems Perspective. 4th edition. Addison-Wesley, Boston, MA, USA,

	2001. J. M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd Edition. Pearson Education, Inc. (Prentice Hall), Upper Saddle River, NJ, USA, 2003. S.-M. Kang, Y. Leblebici. CMOS Digital Integrated Circuits: Analysis and Design. The McGraw-Hill Companies, Inc., New York, NY, USA, 1996. For more details on CMOS digital integrated circuit design. Notes and transparencies by the lecturer on specific topics will also be provided during the course.
Modalità verifica apprendimento	The exam consists in a written examination (exercises) and an oral examination (theory). The exam aims at assessing the skills of the student at the level of both understanding the contents illustrated during the course and designing and/or analyzing simple digital circuits. The planned duration of the written examination is about 2 hours; during this examination, the use of textbooks, notes, and pocket calculators is allowed. The results of the written examination will be provided and discussed in a classroom, in a date agreed upon with students at the end of the written exam. Relative weight of the two examinations for the final mark: written examination 1/2, oral examination 1/2.
Altre informazioni	
Obiettivi Agenda 2030 per lo sviluppo sostenibile	Gli obiettivi