UNIVERSITÀ DI PAVIA

Anno Accademico 2019/2020

ANALOG INTEGRATED CIRCUITS

Anno immatricolazione	2019/2020
Anno offerta	2019/2020
Normativa	DM270
SSD	ING-INF/01 (ELETTRONICA)
Dipartimento	DIPARTIMENTO DI INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE
Corso di studio	ELECTRONIC ENGINEERING
Curriculum	Microelectronics
Anno di corso	1°
Periodo didattico	Primo Semestre (30/09/2019 - 20/01/2020)
Crediti	9
Ore	88 ore di attività frontale
Lingua insegnamento	English
Tipo esame	ORALE
Docente	BONIZZONI EDOARDO (titolare) - 9 CFU
Prerequisiti	Although in the introductory part of the course these concepts will be recalled, to effectively follow the course, it is required the basic knowledge on MOS transistor theory.
Obiettivi formativi	After having recalled the MOS transistor physics and theory, the course describes the design techniques of analog integrated circuits and teaches how to properly design CMOS operational amplifiers and comparators for mixed analog-digital integrated systems. In addition, the course covers and explains layout techniques specific for analog circuits. The described circuits are the basis of signal processing systems for a variety of electronic applications. The objectives of the course include, in addition to the theoretical study, the use of CAD design tools normally used in the profession as a designer of integrated circuits. At the end of the course, the student will have learnt the basic analog building block schemes, how to connect them to achieve more complicated functions

	(operational amplifiers, voltage comparators, bandgap circuits), layout techniques specific for analog circuits, usage of professional CAD tools.
Programma e contenuti	- The MOS transistor: review of its properties and I-V characteristics, CMOS technology, equivalent circuits, noise, and layout. - Integrated resistors, capacitors, and switches: accuracy, issues, and layout techniques. - Design of basic building blocks: inverter with active load, cascode, cascode with cascode load, differential stage, source follower, threshold independent level-shift, improved output stages. - Current and voltage sources: current mirrors, current references, voltage biasing, voltage references. - CMOS operational amplifiers: general design issues and performance characteristics, basic architecture, two-stage amplifiers (differential gain, common mode gain, offset, frequency response and compensation, slew rate), single stage schemes (telescopic, mirrored, folded, single stages with enhanced DC gain), class AB amplifiers, fully differential amplifiers. - CMOS voltage comparators: general design issues and performance characteristics, offset compensation, latches. - Basics on power conversion: overview on voltage regulation, buck and boost DC-DC converters, control loops, single-inductor multiple-output converters.
Metodi didattici	Lectures (hours/year in lecture theatre): 58 Practical class (hours/year in lecture theatre): 30. Lectures use electronic presentations, supported by additional explanations and numerical examples at the blackboard. The individual practical activities consist in designing and simulating at the transistor level basic analog building blocks by means of professional CAD tools.
Testi di riferimento	- F. Maloberti, "Analog Design for CMOS VLSI Systems", Kluwer Academic Publishers, 2001.
Modalità verifica apprendimento	The final exam consists of an oral discussion and the final remark is expressed on a scale of 30. During the course, to each student will be assigned a design project that will be presented and discussed at the oral examination together with the topics covered during the course. If the student does not prefer to prepare the design project, the final remark will be limited to 26/30.
Altre informazioni	The final exam consists of an oral discussion and the final remark is expressed on a scale of 30. During the course, to each student will be assigned a design project that will be presented and discussed at the oral examination together with the topics covered during the course. If the student does not prefer to prepare the design project, the final remark will be limited to 26/30.
Obiettivi Agenda 2030 per lo sviluppo sostenibile	$lbl_legenda_sviluppo_sostenibile