



# UNIVERSITÀ DI PAVIA

Anno Accademico 2018/2019

## ADVANCED COMPUTER ARCHITECTURE

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| <b>Anno immatricolazione</b> | 2018/2019  |
| <b>Anno offerta</b>          | 2018/2019  |
| <b>Normativa</b>             | DM270  |
| <b>SSD</b>                   | ING-INF/05 (SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI)  |
| <b>Dipartimento</b>          | DIPARTIMENTO DI INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE   |
| <b>Corso di studio</b>       | COMPUTER ENGINEERING   |
| <b>Curriculum</b>            | Computer Science and Multimedia  |
| <b>Anno di corso</b>         | 1°   |
| <b>Periodo didattico</b>     | Primo Semestre (01/10/2018 - 18/01/2019)   |
| <b>Crediti</b>               | 6  |
| <b>Ore</b>                   | 54 ore di attività frontale  |
| <b>Lingua insegnamento</b>   | English  |
| <b>Tipo esame</b>            | SCRITTO E ORALE CONGIUNTI  |
| <b>Docente</b>               | FERRETTI MARCO (titolare) - 6 CFU  |
| <b>Prerequisiti</b>          | Basic understanding of computer architecture and assembly language. The C-language is required for the programming lab and associated project.   |
| <b>Obiettivi formativi</b>   | The course describes the architecture of modern processors and multi-processors and introduces the principles of parallel programming. The student will understand the principle of operation of current processors and will be able to assess the distinctive features of general purpose vs embedded microprocessors. The emerging multi-core paradigm and the associated shared-memory architecture will be discussed and will be the basis for a parallel programming project following the OpenMP standard. |
| <b>Programma e contenuti</b> | The course is split into two major areas: a description of the architectures and a laboratory on parallel programming.   |

## The processor

This part of the course introduces the basic concepts underlining the design of modern processors

## The Instruction Set Architecture (ISA)

A Taxonomy for ISAs: CISC, RISC, general purpose, embedded, multimedia

## Processor Implementation

The architecture of a uni-processor, in all its possible implementations, to support both general purpose and embedded processing.

Basic pipelining: control, hazards, exceptions

Superscalar pipelines: static multiple issue, the VLIW approach

Dynamic scheduling, speculative execution, predicate execution (hints)

Compiler support and software optimization

## Caches and memory hierarchy

A description of caches and their hierarchy, excluding virtual memory.

Memory hierarchy and caches: locality

Structure and organization: direct mapping, associativity

Pipelined and multi-level caches

Streaming buffer and multimedia requirements

## Multi-processors

A review of multi-processors and parallel architectures, with emphasis on multi-core processors.

Parallel processing: SIMD, MIMD, data parallelism, thread parallelism, coarse-grain parallelism

Parallel architectures: shared-memory, distributed memory, clusters

Cache coherency and memory consistency

Synchronization

## Parallel programming

An introduction to parallel processing, with hands-on lab on OpenMP.

The available paradigms: SMP, MPI, graphics and CUDA

The OpenMp standard

### Metodi didattici

Lectures (hours/year in lecture theatre): 32

Practical class (hours/year in lecture theatre): 22

Practicals / Workshops (hours/year in lecture theatre): 0

Lectures are delivered through presentations posted on the course web site.

### Testi di riferimento

J. L. Hennessy & D. A. Patterson. Computer Architecture: A Quantitative Approach, 3rd - 4th and 5th editions. Elsevier - Morgan Kaufmann. See detailed instructions on the course website for editions and chapters to be used..

D. A. Patterson & J. L. Hennessey. Computer Organization and Design:

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|  | <p>The Hardware/Software Interface, Revised 4th Edition. Morgan Kauffman. See detailed instruction in the Course website for chapters to be used.</p> <p>M. Ferretti, D. Gunetti. Course charts (in pdf). available for download form the course website</p> |
| <b>Modalità verifica apprendimento</b>                   | The final assessment is composed of a parallel programming project, of a discussion of the project and of a written test (oral examination is optional).   |
| <b>Altre informazioni</b>                                | The final assessment is composed of a parallel programming project, of a discussion of the project and of a written test (oral examination is optional).   |
| <b>Obiettivi Agenda 2030 per lo sviluppo sostenibile</b> | <a href="#">\$bl legenda sviluppo sostenibile</a>  |