UNIVERSITÀ DI PAVIA

Anno Accademico 2017/2018

DIGITAL IC DESIGN

Anno immatricolazione	2017/2018
Anno offerta	2017/2018
Normativa	DM270
SSD	ING-INF/01 (ELETTRONICA)
Dipartimento	DIPARTIMENTO DI INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE
Corso di studio	ELECTRONIC ENGINEERING
Curriculum	Microelectronics
Anno di corso	1°
Periodo didattico	Secondo Semestre (05/03/2018 - 15/06/2018)
Crediti	6
Ore	70 ore di attività frontale
Lingua insegnamento	English
Tipo esame	SCRITTO E ORALE CONGIUNTI
Docente	TORELLI GUIDO (titolare) - 6 CFU
Prerequisiti	Fundamentals of Logic Circuits and Computer Architecture, Basics of Electrical Engineering, Electronics, Basics of Digital Electronics, Basics of CMOS Logic Gates and Integrated Circuit Technology.
Obiettivi formativi	The main objective of the course is to provide the student with the basics of circuit design for combinational and sequential logic in CMOS technology and the operating principles of semiconductor memories. Theoretical lessons will be followed by practical classes in lecture theatre for detailed analysis and exercises, as well as by computer laboratory sessions, during which the student will use SPICE-based computer simulation to analyze basic digital circuit blocks. A few seminars on specific topics will also be provided. At the end of the course, the student is expected to be able to design and analyze basic digital circuit blocks and architectural solutions in CMOS technology as well as to evaluate their performance.

Programma e contenuti	Logic gates in CMOS technology Review of the MOS transistor. Review of inverter and combinational logic gates in CMOS technology. Transistor sizing of CMOS logic gates. Evaluation of rise time, fall time, and delay time of CMOS logic gates. Circuit performance estimation Parasitic electrical parameter estimation (resistance, capacitance, inductance). Distributed RC effects of interconnect lines. Ring oscillator. Speed performance analysis of logic gates. Buffered structure for heavy capacitive loads. Power consumption estimation. Power consumption reduction techniques. Design margins. Sizing of interconnect lines. Pass transistor logic. Shrinking and technology scaling down. Circuit design in CMOS technology Design strategy for combinational logic. Dynamic CMOS logic; precharge logic; domino logic; clocked CMOS logic. Clocked sequential systems. Review of basic static memory elements (latch, flip-flop). Single-phase and two-phase timing. Dynamic memory elements. Synchronous systems. Pipeline architecture. Clock distribution in digital integrated circuits. Clock skew in synchronous systems. Remarks on low-power digital circuit design. Semiconductor memories Introduction to semiconductor memories. Memory types. Organization of a memory. Row and column address circuits. Review of volatile memories (static RAM, dynamic RAM). Non volatile memories: ROM, Flash memory; emerging non volatile memories: phase change memory. Content addressable memory (CAM). Charge pump based integrated voltage elevators.
Metodi didattici	Lectures (hours/year in lecture theatre): 22 Practical class (hours/year in lecture theatre): 30 Practicals/Workshops and Seminars (hours/year in lecture theatre and computer lab): 18
Testi di riferimento	N. H. E. Weste, K. Eshraghian . Principles of CMOS VLSI Design. A System Perspective. 2nd edition. Addison-Wesley Publishing Company, Reading, MA, USA, 1994. N. H. E. Weste, D. M. Harris. CMOS VLSI Design. A Circuits and Systems Perspective. 4th edition. Addison-Wesley, Boston, MA, USA, 2001. J. M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd Edition. Pearson Education, Inc. (Prentice Hall), Upper Saddle River, NJ, USA, 2003. S.-M. Kang, Y. Leblebici. CMOS Digital Integrated Circuits: Analysis and Design. The McGraw-Hill Companies, Inc., New York, NY, USA, 1996. For more details on CMOS digital integrated circuit design.
Modalità verifica apprendimento	Written examination (exercises) and oral examination (theory). Relative weight: written examination 1/2, oral examination 1/2.

Altre informazioni	Written examination (exercises) and oral examination (theory). Relative weight: written examination 1/2, oral examination 1/2.
Obiettivi Agenda 2030 per lo sviluppo sostenibile	$lbl_legenda_sviluppo_sostenibile