UNIVERSITÀ DI PAVIA

Anno Accademico 2021/2022

DIGITAL DESIGN

Enrollment year	2020/2021
Academic year	2021/2022
Regulations	DM270
Academic discipline	ING-INF/05 (DATA PROCESSING SYSTEMS)
Department	DEPARTMENT OF ELECTRICAL,COMPUTER AND BIOMEDICAL ENGINEERING
Course	ELECTRONIC AND COMPUTER ENGINEERING
Curriculum	PERCORSO COMUNE
Year of study	2°
Period	2nd semester (07/03/2022 - 17/06/2022)
ECTS	6
Lesson hours	50 lesson hours
Language	Italian
Activity type	WRITTEN AND ORAL TEST
Teacher	TORTI EMANUELE - 6 ECTS
Prerequisites	The topics of the course presupposes the knowledge of the concepts faced during the "fondamenti di informatica" course.
Learning outcomes	This course is meant to address the fundamentals of Boole's algebra, the methods and the techniques of Analysis and Design of the Logic Networks, both combinatorial and sequential, (asynchronous and synchronous) and a description of the functions of the Arithmetic/Logic Unit in the scenario of the architecture of a numeric processor. The VHDL language is introduced. The student will learn to understand the functions of the Arithmetic/Logic Unit and its performances and to describe simple circuits in VHDL language.
Course contents	Introduction to Boole's Algebra Introduction to Logic and Set Theory; Boole's Algebra; boolean

	expressions and functions; consensus theorem; canonical forms; implicants and implicates; representation of boolean functions; simplification of boolean functions and minimum cost functions, delay of a logic gate. Combinatorial networks Combinatorial networks; logic variables and electrical signals; elementary electronic components; elementary functional blocks: And, Or, Not, Nor, Nand, Xor, Analysis of Combinatorial networks; Synthesis of Combinatorial networks. Elementary Combinatorial networks: coder, decoder, multiplexer, adder, multiplier and divider for constant values. Sequential networks Sequential networks: internal state; finite state machines, minimum machines. Analysis of sequential machines, temporal analysis. Remarkable Sequential networks: Latch and Flip–Flops, registers, counters, sequence detectors, serial and parallel adders. Synthesis of sequential machines. VHDL language Introduction to VHDL language; description of combinatorial networks in VHDL; description of sequential networks in VHDL; simulation and test of logical circuits.
Teaching methods	Logical Network Module: Lectures (hours/year in lecture theatre): 37,5 Practical class (hours/year in lecture theatre): 12,5 Practicals / Workshops (hours/year in lecture theatre): 0
Reccomended or required readings	M. Morris Mano, Charles R. Kime, T. Martin, “Logic and Computer Design Fundamentals” Pearson Education, 2016, V edition.
Assessment methods	The exam of the Logical Network module consists of a written test followed by the chance to sustain an oral examination to improve the final rank. The topic of the oral exam is the VHDL language.
Further information	
Sustainable development goals - Agenda 2030	$lbl_legenda_sviluppo_sostenibile